

Appl. No: 09/410,974  
Amdt. Dated Aug. 16, 2004  
Reply to Office action of June 15, 2004

### REMARKS/ARGUMENTS

Claims 1, 3-10 and 12-20 remain in the application. Claims 2 and 11 were previously cancelled.

#### A. Rejections under 35 U.S.C. 103.

Claims 1, 3, 4, 6, 7, 9, 10, 12-14, 16, 17, and 19 were rejected under 35 U.S.C. 103 based upon Carson et al. in view of Katzman et al. This rejection is respectfully traversed.

Independent claims 1, 6 and 7 call for, among other things, a plurality of functional modules formed within an integrated circuit that are interconnected via a packet router that is also formed within the integrated circuit. At least these features of claims 1, 6 and 7 are not shown or suggested by the relied on references.

It appears that the Office Action acknowledges that Carson et al. and Katzman et al. show systems that involve multiple, separate integrated circuits and use packet communication to exchange messages between the separate integrated circuits. A significant feature of the claimed invention is the implementation of routed, packet communications within an integrated circuit between functional modules on that integrated circuit.

The Office Action argues that "Carson anticipates that the invention may be exemplified by an integrated circuit" because Carson is an improvement on the Intel 82C59A and/or 82480 chips. This assertion, however, is not supported in the references themselves. First, the Intel 82C59A and/or 82480 were marketed as members of "chip sets", not stand-alone integrated circuits. Second, nothing in the Carson or Katzman or any other cited references suggests that the Intel 82C59A and/or 82480 used packet communication between functional modules of the Intel 82C59A and/or 82480 integrated circuits. Fig. 1 in Carson seems to overcome this suggestion in the Office Action in that it does not show or suggest modules that are interconnected by a packet router,

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nor does Fig. 1 show even a packet router, or packet handling circuitry. Hence, Carson and Katzman taken alone or in combination suggest, at most, the conventional use of packet communication between separate integrated circuits.

The Office Action states at three locations, without authority, a proposition that "it is generally considered to be within the ordinary skill in the art to shift the location of parts...." However, this bald statement is not supported by any reference to authority, and is contrary to the instruction of MPEP 2144.04 (VI)(C). In this section of the MPEP, entitled "Rearrangement of Parts", it is noted that "the mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims...is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason...to make the necessary changes..." In this case the Office Action fails to state any motivation for making the suggested change.

More fundamentally, the Office Action fails to even state what parts of the reference would be rearranged to meet the limitations of claims 1, 6 and 7. Is one supposed to rearrange the processors in Fig. 2 and place them inside the MPIC controller 100 along with MPIC Bus 103? If so, where is there any suggestion to make such a change? What is the motivation to make such a change? Where is there any indication of an expectation of success in making such a change? Clearly, the Office Action fails to state even a *prima facie* case of obviousness.

It is believed that it would take much more than mere rearrangement to transform the teachings of Carson and Katzman so as to meet the limitations of claims 1, 6 and 7. It is more appropriate to consider the instruction found at MPEP 2144.04 (V)(B) entitled "Making Integral". Here the MPEP sets out that integrating components into an integral mechanism is not, *per se*, obvious. See, *Schenck v. Nortron Corp.*, 218 USPQ 698 (Fed. Clr. 1983).

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Accordingly, claims 1, 6 and 7 as well as claims 3, 4 and 17 that depend from them, are believed to be allowable over Carson et al. in view of Katzman et al.

Independent claim 9 calls for, among other things, an initiator functional module wherein both the initiator functional module and the packet router are formed within the integrated circuit. Similarly, independent claim 10 calls for a target functional module wherein both the target functional module and the packet router are formed within the integrated circuit. These features of claims 9 and 10 are not shown or suggested in the relied on reference. As noted above, Carson et al. in view of Katzman et al. relate exclusively to multi-chip computer systems and do not show or suggest a packet communication system within an integrated circuit. Only applicant teaches and claims the integration of these features in the particular manner set out in claims 9 and 10. For at least these reasons claims 9 and 10 are not anticipated or made obvious by the relied on references.

Independent claim 12 calls for, among other things, a method of implementing transactions between an initiator module within the integrated circuit, and generating a request packet within said integrated circuit. Carson et al. and Katzman et al. do not show or suggest a method of implementing transactions within an integrated circuit, only transactions external to the integrated circuits and conducted between separate integrated circuits. For at least these reasons claim 12 is not anticipated or made obvious by the relied on references. Claims 13-14, 16 and 19 that depend from claim 12 are believed to be allowable for at least the same reasons as claim 12.

Claims 5, 8, 15, 18 and 20 were rejected under 35 U.S.C. 103 based upon Carson et al. in view of Katzman et al. and further in view of Circello. This rejection is respectfully traversed. Claims 5 and 18, which depend from claim 1, claim 8, which depends from claim 7 as well as claims 15 and 20 which depend from 12 are distinct from the combination of Carson and Katzman for at least the

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same reasons as claims 1, 7 and 12. Circello does not supply the deficiencies set out above. Specifically, Circello does not show or suggest functional modules within an integrated circuit that are coupled by a packet router, nor functional modules within an IC that have packet handling circuitry for communicating with other functional modules within the same IC, nor the implementation of target and initiator functional modules. For at least these reasons, claims 5, 8, 15, 18 and 20 are neither anticipated nor made obvious by Carson et al., Katzman et al. and Circello either alone or in combination.

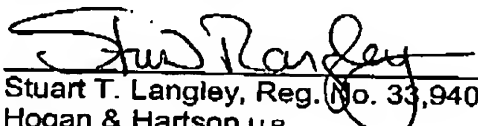
**B. Conclusion.**

In view of all of the above, claims 1, 3-10 and 12-20 are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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